**EXPERIMENT 2**

**Aim:**

Write a program in ARM Assembly language to load any register with 32 bit data and perform following

1. Shift left by 2 bits.
2. Shift right by number of bits stored in register.
3. Shift left 5 bits conditionally when ‘0’ flag is set.
4. Arithmetic shift by the value contained in register.

**Tool used:** Keil uVision4

**Theory:**

Here I have used LSL, LSR and ASR for shifting the bits. LSL is used for shifting the bits left and concatenate a 0 at the LSB. LSR is used for shifting the bits right and concatenate a 0 at the MSB. ASR is used to shift the bits right and concatenate the value of MSB at the new MSB

1. **Shift left by 2 bits.**

**Code:**

 AREA PROGRAM, CODE, READONLY

 ENTRY

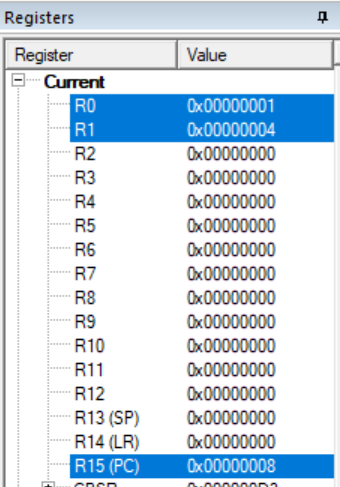
MAIN

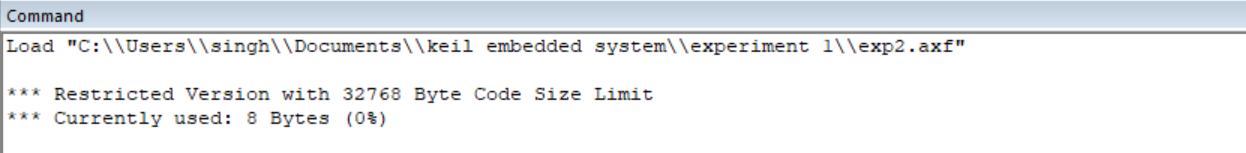
 LDR R0,=0x00000001 ;LOAD R0 with a value

 MOV R1,R0,LSL#0x02 ;move value of R0 to R1 with left shift by 2 bits

 END

**Register Output:**

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1. **Shift right by number of bits stored in register.**

**Code:**

 AREA PROGRAM, CODE, READONLY

 ENTRY

MAIN

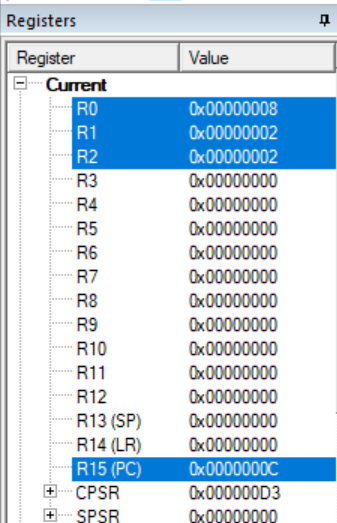
 LDR R0, =0x00000008 ;LOAD VALUE 8 TO R0 REGISTER

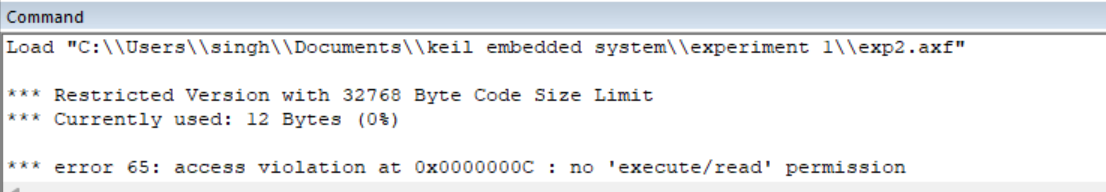
 LDR R1, =0x00000002 ;LOAD THE NO OF TIMES TO BE SHIFTED

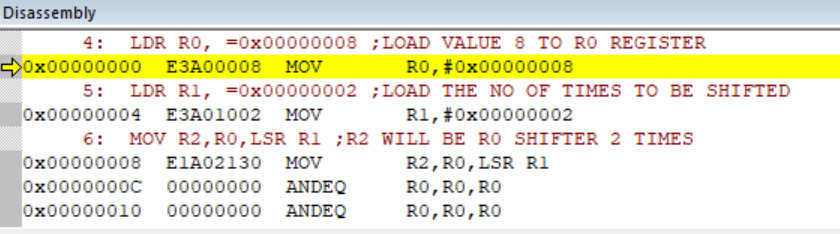
 MOV R2,R0,LSR R1 ;R2 WILL BE R0 SHIFTER 2 TIMES

 END

**Output:**

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1. **Shift left 5 bits conditionally when ‘0’ flag is set.**

**Code:**

 AREA PROGRAM, CODE, READONLY

 ENTRY

MAIN

 LDR R0, =0x00000000 ;LOAD VALUE 0 TO R0 REGISTER

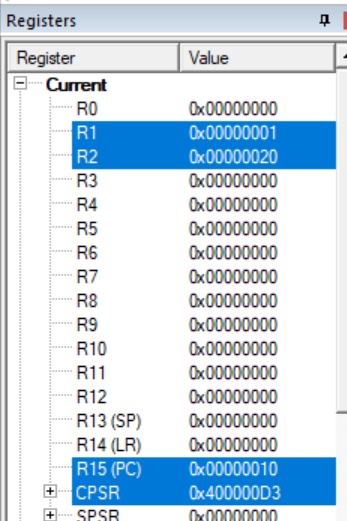
 LDR R1, =0x00000001 ;LOAD VALUE 1 TO R1 REGISTER

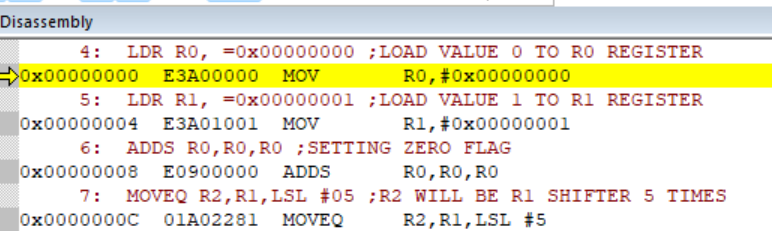
 ADDS R0,R0,R0 ;SETTING ZERO FLAG

 MOVEQ R2,R1,LSL #05 ;R2 WILL BE R1 SHIFTER 5 TIMES

 END

**Output:**

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1. **Arithmetic Shift right by number of bits stored in register.**

**Code:**

 AREA PROGRAM, CODE, READONLY

 ENTRY

MAIN

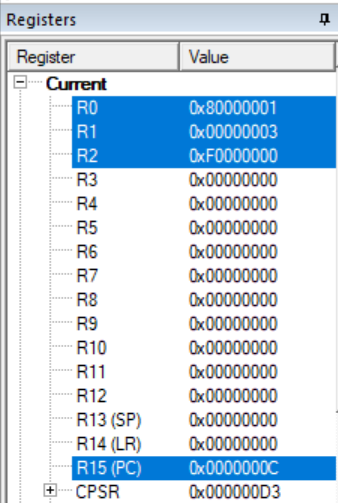
 LDR R0, =0x80000001 ;LOAD VALUE WITH MSB 1 TO R0 REGISTER

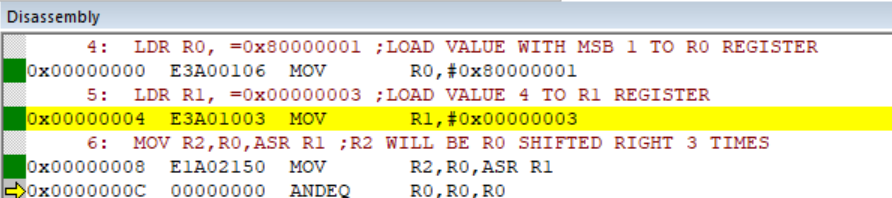
 LDR R1, =0x00000003 ;LOAD VALUE 3 TO R1 REGISTER

 MOV R2,R0,ASR R1 ;R2 WILL BE R0 SHIFTED RIGHT 3 TIMES

 END

**Output:**

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**Result:**

All the parts of the experiments are performed successfully and their results are also verified correctly.